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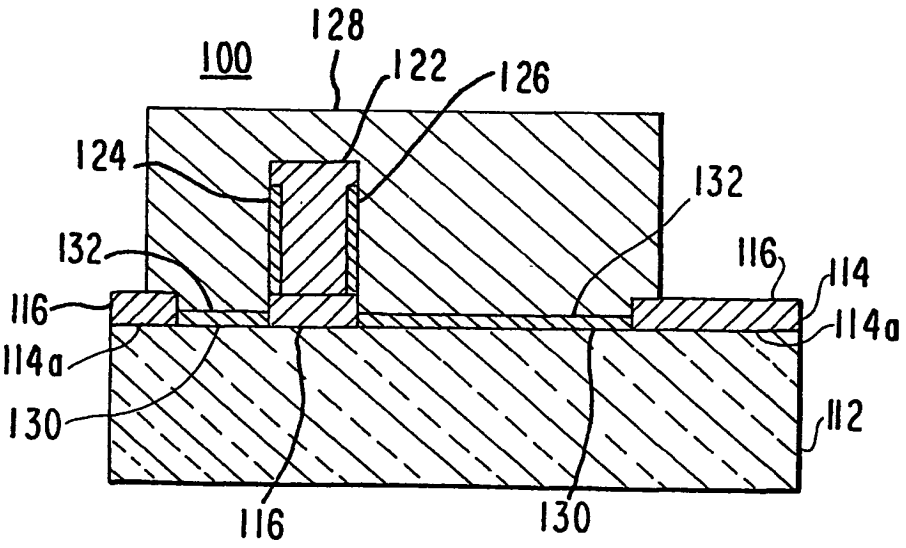
(54) Title: SEMICONDUCTOR MEMORY DEVICE WITH INCREASED NODE CAPACITANCE



(57) Abstract: An integrated circuit semiconductor memory device (100) has a first dielectric layer (116) characterized as the BOX layer absent from a portion (130) of the substrate (112) under the gate of a storage transistor to increase the gate-to-substrate capacitance and thereby reduce the soft error rate. A second dielectric layer (132) having a property different from the first dielectric layer at least partly covers that portion (130) of the substrate. The device may be a FinFET device including a fin (122) and a gate dielectric layer (124, 126) between the gate and the fin, with the second dielectric layer having less leakage than the gate dielectric layer.

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